Datasheet

DB640-17C-A

640x480 LWIR UNCOOLED MICROBOLOMETER

DESCRIPTION

DB640-17C-A is an uncooled infrared image sensor with a reliable, small and lightweight, low input power focal plane array.

SPECIFICATION

- 640x480 pixel focal plane array
- Pixel-pitch : 17 ㎛
- NETD ≤ 50mK @ f/1, 300K, 30 ㎐
- Frame-rate : Max 60 ㎐ @ 2ch
- Video output : 1ch or 2ch (Selectable)
- 1ch max 30 ㎐, 2ch max 60 ㎐
- Default mode : 2ch
- Dimensions (WxHxD) : 24x24x3.3 ㎣ (without pin)
- Weight : ≤7g
- Spectral Response : LWIR
- Sensitive area : 10.88x8.16 ㎟
- Thermal time constant ≤15 ㎳
- Array format windowing capability

FEATURES

- Uncooled operation
- Adjustable integration time
- Power supply: 5V for analog and digital
- Output dynamic range: 1 V to 4 V
- H, V image flip array
- 27-lead ceramic vacuum package
- On-chip temperature sensor
- Typical responsivity : 10 mV/K
- User defined windowing capability

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1. DESCRIPTION

The aim of this document is to explain the main features, performance and specifications of the 640 x 480 pixel uncooled microbolometer named as DB640-17C-A.

DB640-17C-A is an opto-electronic device sensitive to infrared radiation in the long wave spectral range (see Figure 2). It has a microbolometer Focal Plane Array (FPA) made up of 640 x 480 elements, which are two dimensional detector array made from titanium oxide resistive bolometer linked to the silicon Read-Out Integrated Circuit (ROIC). DB640-17C-A infrared image sensor produces raw analog video data at up to 60 frames per second. The sensor could be controlled by a serial communication data input. The pixel size is 17 μm x 17 μm. The image size is 10.88 mm by 8.16 mm with 640 x 480 nominal formats.

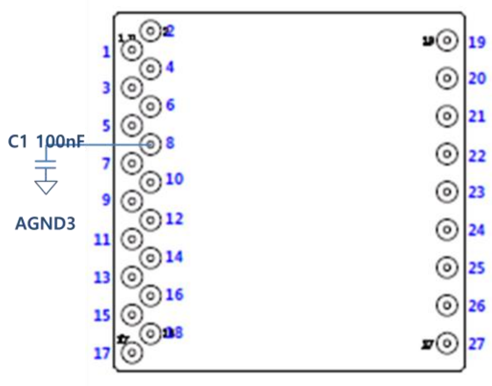


Figure 1 Pinout diagram (rear view)

Pin Number	Name	In/Out	Description
1	OVDD	Input	Output Supply Voltage
2	OGND	Input	Output Ground
3	VOUT_O	Output	Odd Row Output Voltage
4	VOUT_E	Output	Even Row Output Voltage
5	AVDD1	Input	1st Analog Supply Voltage
6	AGND1	Input	1st Analog Ground
7	Reserved	-	-
8	Ref	Input	Analog Ground with 100nF cap (necessary)
9~13	NC	-	-
14	AVDD2	Input	2nd Analog Supply Voltage
15	AGND2	Input	2nd Analog Ground
16	Reserved	-	-
17	Reserved	-	-
18	Reserved	-	-
19	DVDD1	Input	1st Digital Supply Voltage
20	DGND1	Input	1st Digital Ground
21	FSYNC	Input	Frame Sync. Signal
22	LSYNC	Input	Line Sync. Signal, Integration Time Control
23	MCLK	Input	Master Clock
24	DVDD2	Input	2nd Digital Supply Voltage
25	DGND2	Input	2nd Digital Ground
26	CLE	Input	Command Latch Enable
27	SCDI	Input	Serial Communication Data Input

Table 1 Description of pin configuration

2. WARRANTED PARAMETERS

2.1 Electro-optical Performance

2.1.1 Test operating conditions

The test condition of DB640-17C-A is set at a typical background temperature of 20 ± 2°C and the output rate is 10 MHz (for a 30 Hz acquisition frequency). The electro-optical parameters are defined and measured with an f/1.0 optical aperture condition.

The useful temperature dynamic range at the detector window level is higher than 100°C.

2.1.2 Temporal NETD

The average temporal pixel NETD is better than 50mK at a 30 Hz frame rate and the temperature of 293K.

2.1.3 Responsivity

This parameter is not a specification and is given only for information only. For information, the value of responsivity is typically 10mV/K. The responsivity mean value is calculated upon the operating pixel population.

2.1.4 Spectral response

The DB640-17C-A shows a typical spectral response as seen on Figure 2 below.

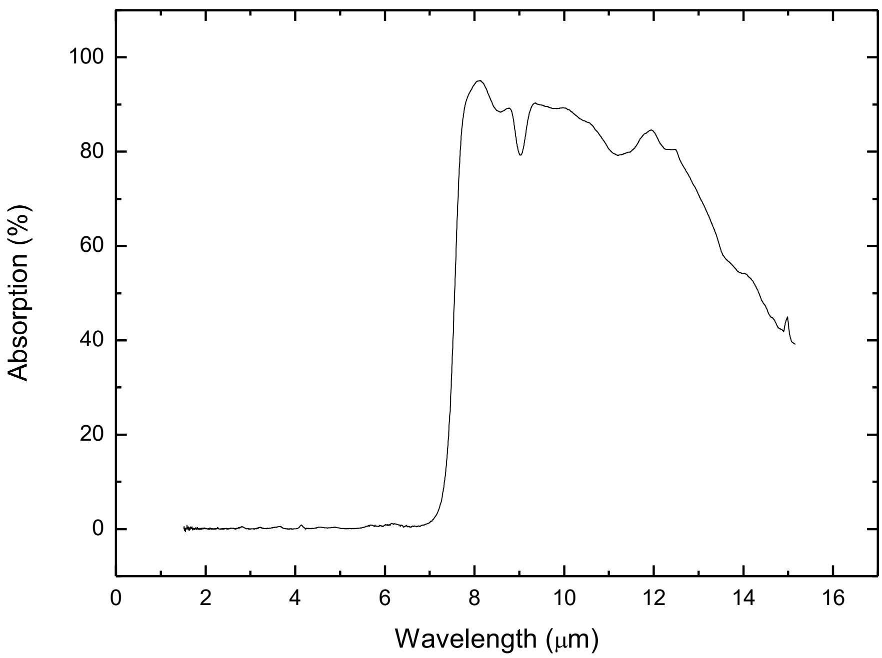


Figure 2 Typical spectral response gauge of DB640-17C-A

	Wavelength	Transmittance
Average Transmittance	8μm ≤ λ ≤ 10 μm	≥ 86%
	8μm ≤ λ ≤ 14 μm	≥ 77%
	1μm ≤ λ ≤ 6.5 μm	≤ 1%
Peak Transmittance	1μm ≤ λ ≤ 6.5 μm	≤ 3%
Cut on wavelength	7.5±0.2 μm	50%

Table 2 Specification of Transmittance

2.2 Defect

2.2.1 Definition

Non-operating pixel
A pixel is referred to "non-operating" if:

- Its responsivity is < 0.7 x average responsivity or > 1.3 x average responsivity
- Its NETD is ≥ 75mK

A single non-operating pixel is a non-operating pixel with no adjacent non-operating pixel.

Areas
The FPA is divided in two areas which have the same optical axis (see figure 3):

- Area A : the central zone of 160 x 120 pixels
- Area B : the 640 x 480 area (i.e. excluding area A) of the array

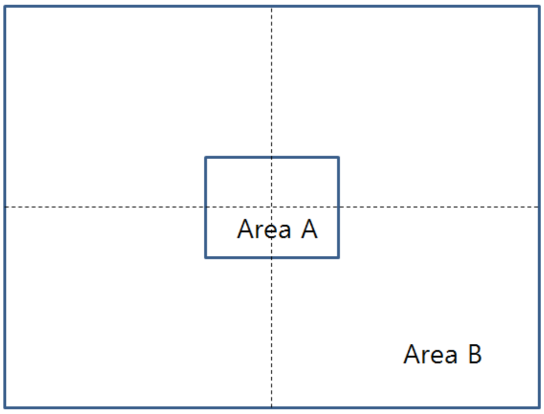


Figure 3 Area definition

Cluster
A cluster is defined as a group of at least two non-operating pixels adjacent by side or corner. The clusters are defined by their size in terms of non-operating pixels.

2.2.2 Operability specification

Operability of the array higher than 99.0% (typically ≥ 99.5%)

Zone	Cluster size
Area A	Maximum cluster size = 8
Area B	≤ 2 clusters of 9 to 14 non-operating pixels maximum Maximum cluster size = 14

Table 3 Operability specification

2.3 Mechanical and Thermal Specification

2.3.1 Weight

The weight of DB640-17C-A is less than 7g.

2.3.2 Total power consumption

The stabilized power consumption of DB640-17C-A at room temperature is less than 350mW at 30Hz frame rate.

3. ENVIRONMENTAL CONDITIONS

A qualification to the following environmental conditions has been performed on detectors taken by sampling into the production deliveries and therefore fully representative of the produced detector quality. These conditions do not represent the maximum detector acceptable levels.

3.1 Climatic Environment

3.1.1 High temperature storage

MIL-STD 810G, method 501.5 : storage 7 days at +63°C

3.1.2 High temperature operation

MIL-STD 810G, method 501.5 : 3 days x 1cycle (1cycle=24hours) at +63°C

3.1.3 Low temperature storage

MIL-STD 810G, method 502.5: storage 72 hours at -32°C

3.1.4 Low temperature operation

MIL-STD 810G, method 502.5 : Maintain -32°C for at least two hours following temperature stabilization and conduct an operational checkout

3.2 Mechanical Environment

3.2.1 Vibration

Composite wheeled vehicle vibration exposure

MIL-STD 810G, method 514.6C-VI. Category 4 : Vertical 2.24grms, Transverse 1.48grms, Longitudinal 1.90grms , 2 hours / axis

Propeller aircraft vibration exposure

MIL-STD 810G, method 514.6D-II. Category 13 : $L_0 = 0.3g^2/Hz$, $f_0 = 133Hz$, 1 hour / axis

Jet aircraft external store vibration exposure

MIL-STD 810G, method 514.6D-IV. Category 15 : $W_1 = 0.0026\ g^2/Hz$, $W_2 = 0.097\ g^2/Hz$, $f_0 = 2000Hz$, $f_1 = 1900Hz$, 30s / axis

3.2.2 Shocks

MIL-STD 810G, method 516.6 Procedure I : saw tooth 20g 11ms, 3 shocks per axis & per direction

4. ELECTRICAL INTERFACES

4.1 Readout Circuit Description

4.1.1 Readout integrated circuit architecture

The CMOS Read-Out Integrated Circuit (ROIC) extracts a signal from a high background current. The ROIC allows the integration of the information from the active cells after subtracting a common background current (skimming function by blind cells), to sample and hold this information row by row and to multiplex the information to the output.

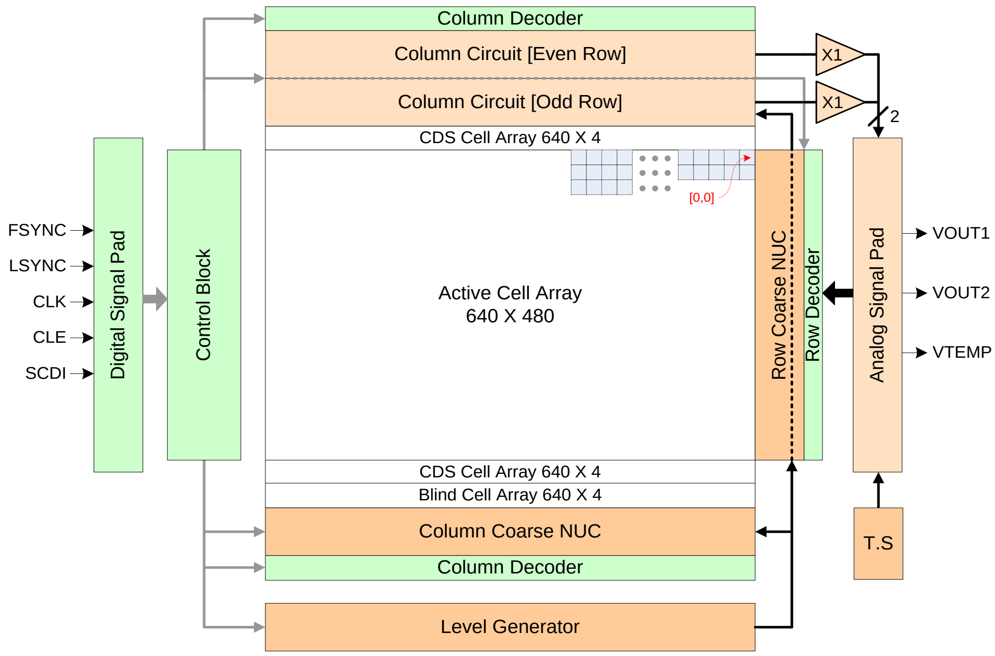


Figure 4 Read-Out Circuit diagram

- Cell array : active cells (640x480), Correlated Double Sampling (CDS) cells (640x4[T], 640x4[B]), blind cells (640x2[Even Row], 640x2[Odd Row]), ATM cells (640x4)
- Column Circuit : integration of signals, CDS, Sample/Hold function
- Coarse Non-Uniformity Correction (NUC) : Resistance non-uniformity correction of the active & blind cell array
- Column & Row Decoder : generation of signals for cell access (windowing capability)
- Control Block : generation of core control signal & level generator control signal
- Level Generator : generation of core bias level & amp bias level
- Output Amp : transmitting the output of column circuit to a analog pad

4.1.2 Operating mode

The standard readout operation of the detector is muti-integraion which read even and odd rows simultaneously. The both rows of V, V+1 integration and both rows of V-2, V-1 readout run simultaneously. The output channel is selectable by resister setting from 1 to 2. (see Figure 8 Output timing diagram : 1 channel vs 2 channel mode.)

4.1.3 Current-voltage conversion

The current is integrated in a current-voltage conversion stage located at the end of each column. The current-voltage conversion is performed by a Capacitance Trans-Impedance Amplifier (CTIA). Integration time and capacitance control is available to optimize a gain.

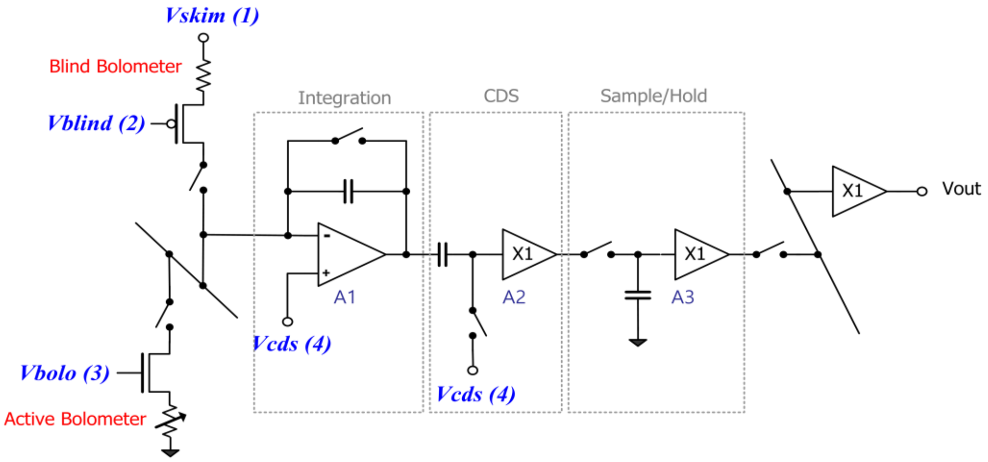


Figure 5 Read-out circuit Schematic

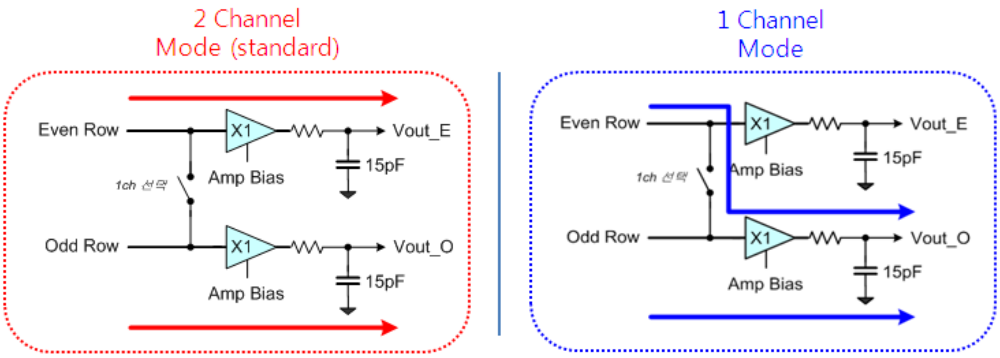


Figure 6 Output channel mode

	Input Range	Output Range
A1	2.0V ~ 3.0V	1.0V ~ 4.0V
A2	1.0V ~ 4.0V	1.0V ~ 4.0V
A3	1.0V ~ 4.0V	1.0V ~ 4.0V

Table 4 Input and Output range of amplifiers

4.1.5 Output stage

After signal current-voltage conversion and sample/hold of even and odd rows, multiplexer (640 to 1) allows signals of both rows to be transferred to 2 channel output or 1 channel output(selectable). The master frequency of the readout circuit (and hence the output rate) is adjusted with respect to the acquisition frequency aimed at.

4.2 Input Interface

Clock frequencies of signals are governed by the Master Clock (MCLK). Control signals necessary to operate the ROIC are :

- MCLK : Master Clock for ROIC operation, Tclk = 1period time of MCLK
- FSYNC : Frame sync for ROIC operation, it determine a frame rate
- LSYNC : Line sync for ROIC operation, it determine a integration time
- CLE : Command Enable signal for ROIC control
- SCDI : Data signal for ROIC control

4.2.1 Timing Diagram

1 period of LSYNC is consist of Integration Time and dummy clock.

- Integration time : Tpw – 20Tclk
- Dummy clock : needs to be longer than a specific time to prevent from output overlay
- LSYNC to 1st Column output : 36.5Tclk

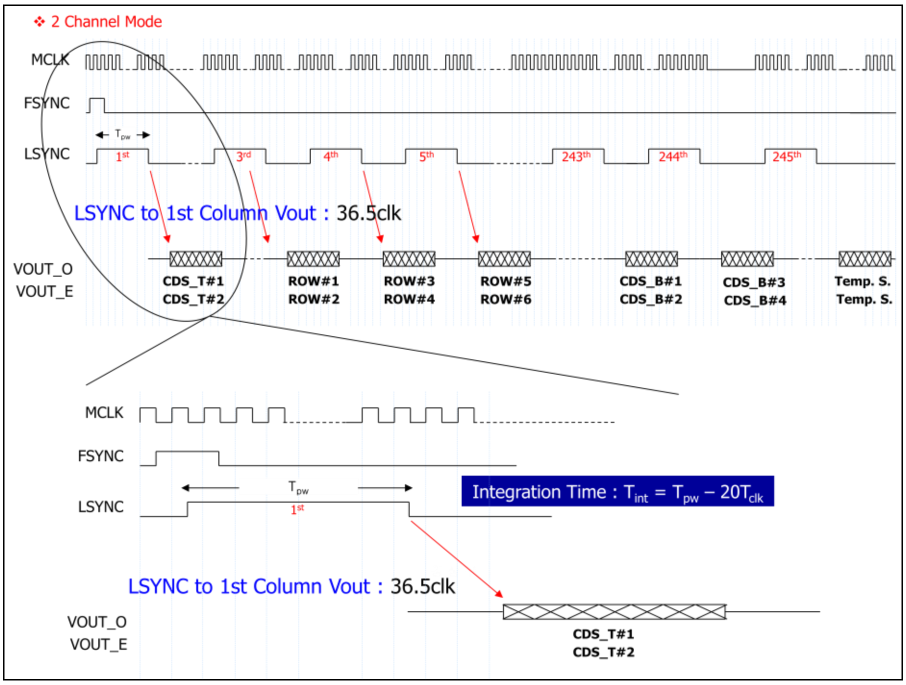


Figure 7 Output timing diagram

Channel mode is selectable by resister setting (see 4.2.2). The default mode is 2 channel which is better for high frame rate (up to 60Hz)

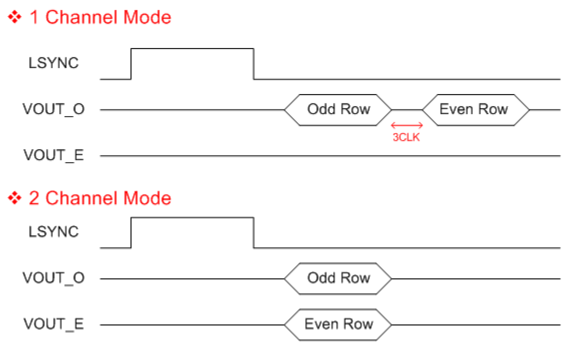


Figure 8 Output timing diagram : 1 channel vs 2 channel mode

4.2.2 Resister Setting

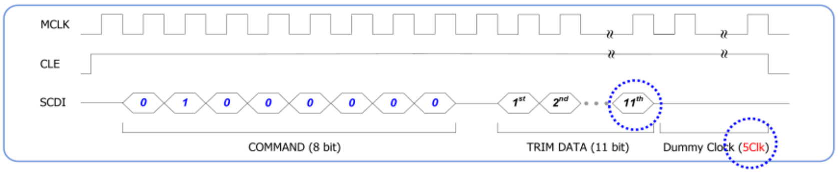
SCDI is composed of command, data and dummy clk. To active SCDI, CLE signal synchronized with a falling edge of MCLK needs to be a high level. The commands for several functions are described below.

Command (8bit)	Function	Data bit (bit)	Resolution	Range	Default (bit)	Analog Level	Dummy CLK	Memo
02h	Vskim level set	11	2.5 mV	1~5 V	01010110000	4.00 V	5	-
03h	Vbolo level set	11 +(1clk) 11	2.5 mV	1~5 V	01011100100	2.85 V	1	Low (for NUC)
					01110011000	3.30 V	5	High (for adjusting a level) recommended bias (3.3V)
04h	Vblind level set	11 +(1clk) 11	2.5 mV	1~5 V	00011011100	1.55 V	1	Low (for NUC)
					00100011000	1.70 V	5	High (for adjusting a level)
05h	Vcds level set	9	10 mV	1~5 V	010000010	2.30 V	7	-
14h	Amp bias level set	12	±30% step	1.6uV ~ 30uV	100011	5 uA	4	MSB 6bit, recommended bias (5uA)
				37.5uV ~ 525uV	011001	375 uA		LSB 6bit, recommended bias (375uA)
0Dh(Even Row), 1Dh(Odd Row)	Column Coarse NUC level set	2560 (: 640 x 4bit)	-	-	1111…..1111	-	16	Vblind Level set between Low(0000) to High (1111), factory supply with each detector
0Eh (Row direction)	Row Coarse NUC level set	1952 (: 488 x 4bit)	-	-	1111…..1111	-	16	Vbolo Level set between Low(0000) to High (1111), factory supply with each detector
0Fh	Int cap 2pF	16bit	-	-	0	-	4	Default integration cap : 6pF
	Int cap 4pF				0			
	Int cap 6pF				1			
	Int cap 1st 8pF				0			
	Int cap 2nd 8pF				0			
	-				0			
	-				0			
	Blind Repair_O				0			Odd Blind cell replacement

	Blind Repair_E				0			Even Blind cell replacement
	-				0			
	-				0			
	-				0			
	-				0			
	-				0			
	-				0			
	-				0			
15h	Row Read direction set	16bit	-	-	1	-	6	0 : Down to up, 1 : Up to down
	Col Read direction set				1			0 : Left to right, 1 : Right to left
	-				0			-
	Top CDS off				0			0 : on, 1 : off
	Bottom CDS off				0			0 : on, 1 : off
	-				**1**			-
	-				0			-
	-				0			-
	-				0			-
	-				0			-
	-				0			-
	-				0			-
	Temp row output				0			0 : on, 1 : off (On chip temp sensor)
	Channel selection				0			0 : 2channel , 1 : 1channel
	-				0			-
	-				1			-
16h	Col Address set	20bit	1 line / 1bit	1 ~ 640	0000000000	1	4	MSB 10bit
					0000000101	640		LSB 10bit
17h	Row Address set	20bit	1 line / **2bit**	1 ~ 480	0000000000	1	4	MSB 10bit
					0000011110	480		LSB 10bit
Reset	DFF & Latch Reset						2	

Table 5 SCDI data Table

- Function of setting the output of Vskim level generator

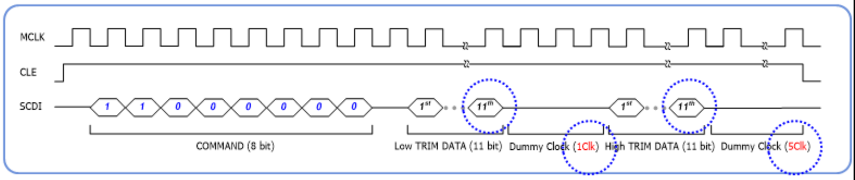
Command	02h
Specification	Range : 1V ~ 5V, Resolution : 2.5mV (11bit)
Timing	

Default

Value	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th
1.00V	0	0	0	0	0	0	0	0	0	0	0
1.01V	0	0	1	0	0	0	0	0	0	0	0
1.02V	0	0	0	1	0	0	0	0	0	0	0
⋮											
4.00V	0	0	0	0	1	1	0	1	0	0	1
⋮											
5.00V	0	0	0	0	0	1	0	0	0	1	1

Figure 9 Vskim latch set mode

- Function of setting the output of Vbolo level generator

Command	03h
Specification	Range : 1V ~ 5V, Resolution : 2.5mV (11bit)
Timing	

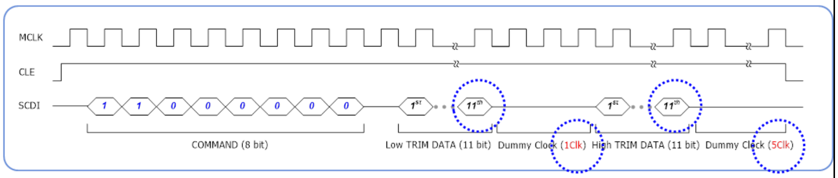
Low Default

High Default

Value	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th
1.00V	0	0	0	0	0	0	0	0	0	0	0
⋮											
2.85V	0	0	1	0	0	1	1	1	0	1	0
⋮											
3.30V	0	0	0	1	1	0	0	1	1	1	0
⋮											
5.00V	0	0	0	0	0	1	0	0	0	1	1

Figure 10 Vbolo latch set mode

- Function of setting the output of Vblind level generator

Command	04h
Specification	Range : 1V ~ 5V, Resolution : (High – Low)/ (2^4-1)mV (Effectively 15bit)
Timing	

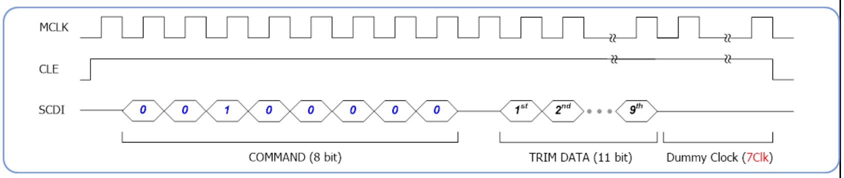
Low Default

High Default

Value	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th
1.00V	0	0	0	0	0	0	0	0	0	0	0
⋮											
1.55V	0	0	1	1	1	0	1	1	0	0	0
⋮											
1.70V	0	0	0	1	1	0	0	0	1	0	0
⋮											
5.00V	0	0	0	0	0	1	0	0	0	1	1

Figure 11 Vblind latch set mode

- Function of setting the output of Vcds level generator

Command	05h
Specification	Range : 1V ~ 5V, Resolution : 10mV (9bit)
Timing	

Default

Value	1st	2nd	3rd	4th	5th	6th	7th	8th	9th
1.00V	0	0	0	0	0	0	0	0	0
1.01V	1	0	0	0	0	0	0	0	0
1.02V	0	1	0	0	0	0	0	0	0
⋮									
2.30V	0	1	0	0	0	0	0	1	0
⋮									
5.00V	0	0	0	1	0	0	0	1	1

Figure 12 Vcds latch set mode

- Function of coarse non-uniformity correction (NUC) mode in column lines

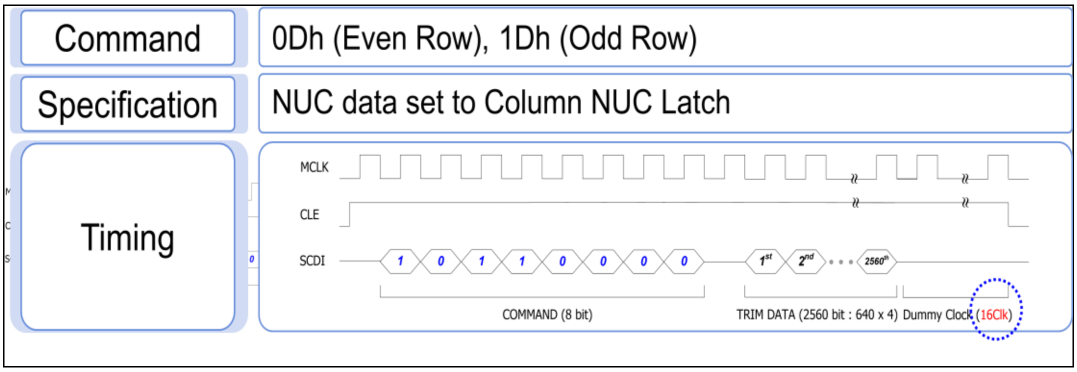


Figure 13 Coarse NUC mode (I)

- Function of coarse non-uniformity correction (NUC) mode in row lines

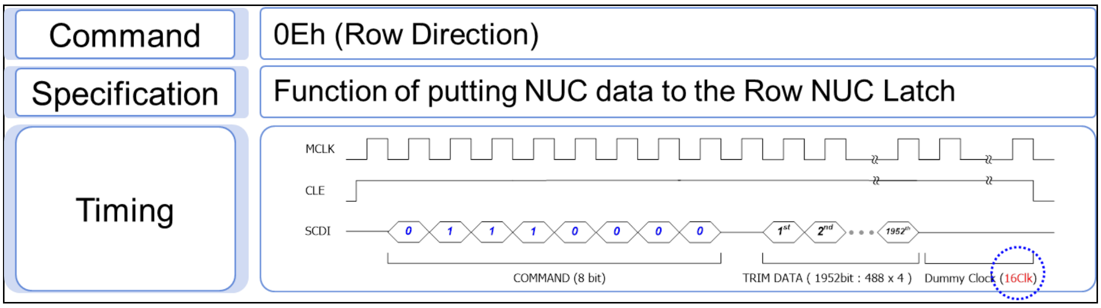


Figure 14 Coarse NUC mode (II)

- Function of setting several Trim information

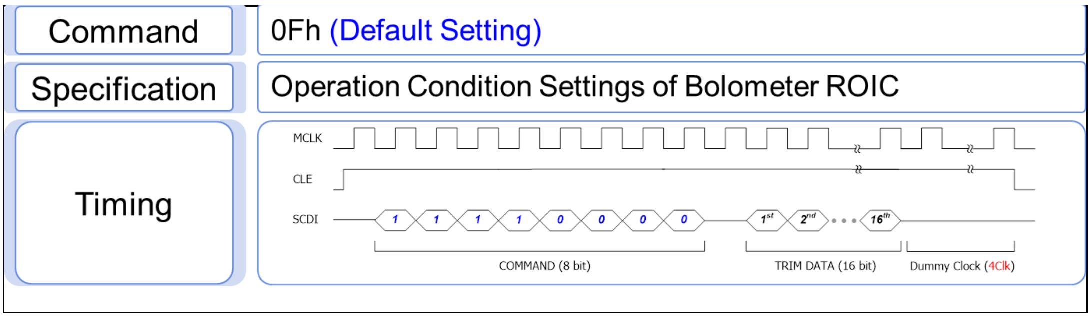
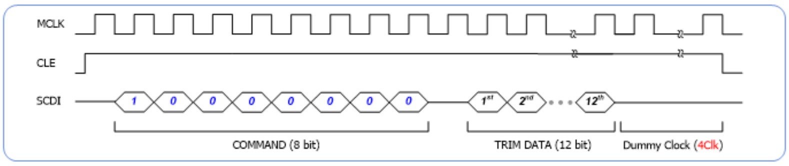


Figure 15 Trim set mode (I)

- Function of setting the value for Amp bias

Command	14h
Specification	- Small Current Block → Range : 1.6uA ~ 30uA, Resolution : ±30% Step - Large Current Block → Range : 37.5uA ~ 525uA, Resolution : ±30% Step
Timing	

Value	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	Value
2.5uA	1	0	0	0	1	0	0	0	0	0	0	1	75uA
3.3uA	0	1	0	0	1	0	1	0	0	0	1	0	112.5uA
4uA	0	1	1	0	1	1	0	0	1	0	0	0	150uA
5uA	**1**	**0**	**0**	**0**	**1**	**1**	**0**	1	0	0	1	0	187.5uA
10uA	0	1	0	0	1	1	0	1	0	0	0	1	225uA
15uA	1	1	0	0	1	1	**0**	**1**	**1**	**0**	**0**	**1**	**375uA**
20uA	0	1	1	0	1	1	**0**	**0**	**1**	**1**	**0**	**1**	**525uA**

Default (5uA row, 1st–6th bits)
Default (375uA row, 7th–12th bits)

Figure 16 Amp bias latch set mode

- Function of setting several Trim information

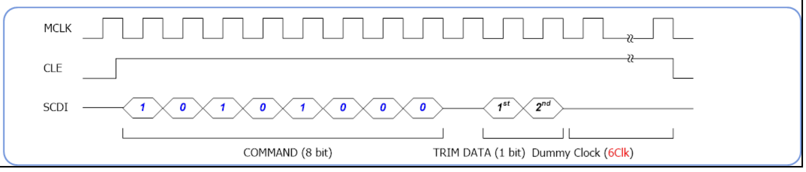
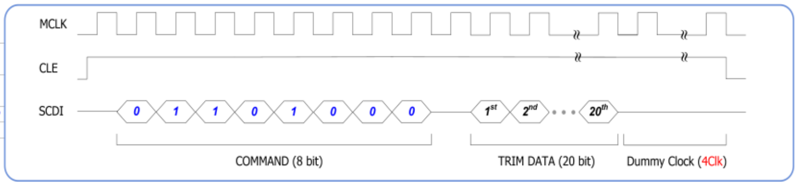
Command	15h (Default Setting & New Trimming Set)
Specification	Bolometer ROIC의 각종 Operation Condition Setting
Timing	

Figure 17 Trim set mode (II)

- Function of setting column start/end address (1 to 640)

Command	16h
Specification	Column Start/End Address Setting by 1bit step
Timing	

Start Default

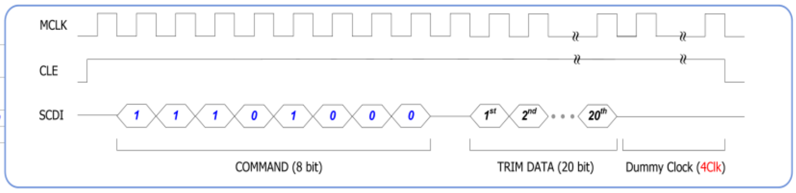
End Default

Start Add	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	End Add
1st Col.	0	0	0	0	0	0	0	0	0	0	Invalid
⋮											
33th Col.	0	0	0	0	0	1	0	0	0	0	32th Col.
⋮											
353th Col.	0	0	0	0	0	1	1	0	1	0	352th Col.
⋮											
Invalid	0	0	0	0	0	0	0	1	0	1	640th Col.

* Start Address : Setting Value + 1, End Address : Setting Value

Figure 18 Column address set mode

- Function of setting row start/end address (1 to 480)

Command	17h
Specification	Row Start/End Address Setting by 2bit step
Timing	

Start Default

End Default

Start Add	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	End Add
1st Col.	0	0	0	0	0	0	0	0	0	0	Invalid
⋮											
25th Col.	0	0	0	1	1	0	0	0	0	0	24th Col.
⋮											
265th Col.	0	0	0	1	0	0	0	0	1	0	264th Col.
⋮											
Invalid	0	0	0	0	0	1	1	1	1	0	480th Col.

* Start Address : Setting Value + 1, End Address : Setting Value

Figure 19 Row address set mode

- Function of generating the DFF and Latch reset pulse

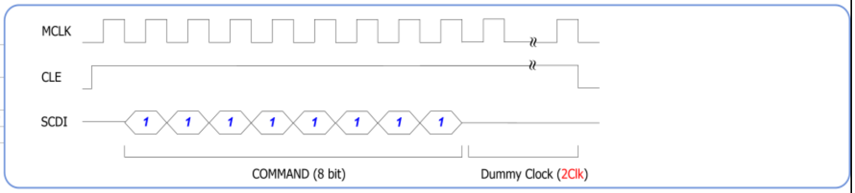
Command	FFh
Specification	Reset DFF & Latch value to Default
Timing	

Figure 20 Function for Reset

4.3 Coarse Non-uniformity Correction

4.3.1 Coarse non-uniformity correction (NUC)

Though default NUC bias level set(resister bit 1111…1111) is still available for operating detector, controlling the bias generator individually to reduce a non-uniformity results in maximizing a dynamic range. **NUC table (resister bit) will be supplied with each detector**. The NUC method described below is only given for information.

- NUC Resolution
  - High Level & Low Level : 1V ~ 5V (Minimum Step : 2.5mV, 11bit), adjustable
  - NUC Level : (High Level – Low Level) / (2^4 - 1)
  - Effectively 15bit (11bit / 4bit) resolution

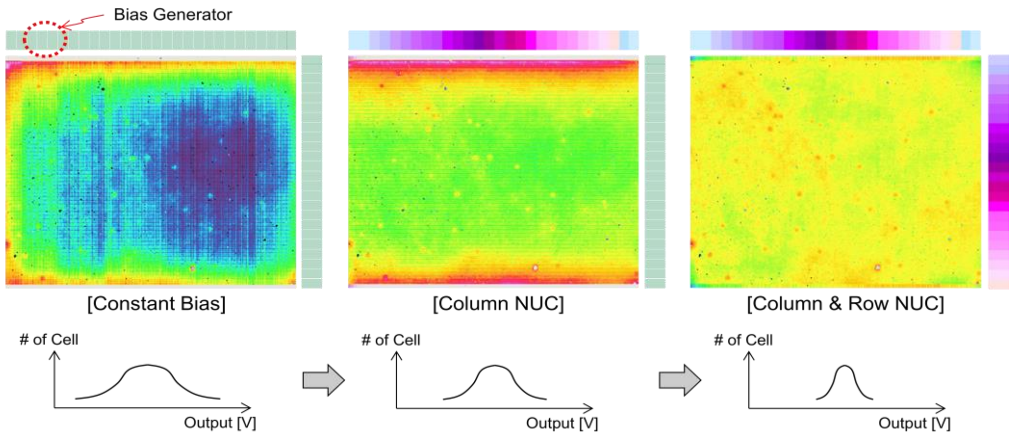


Figure 21 Output signal transition after coarse NUC process

4.3.2 Coarse NUC setting (recommended method)

Process for coarse NUC is divided into the following three steps.

First, set up the average output voltage as changing the value of Vskim and determine a suitable Vskim, which Vout is the nearest to DR/2(tunable value)

Second, confirm a Vblind bias range which is applied to 640 Vblind individually. The bias range is divided into 16 levels. Select one of the 16 levels (0 to 15), which makes the average of Column values close to the average of DR/2. 640 values of Column NUCs are then determined accordingly.

Third, Row NUCs are determined using same process as Column NUCs. 480 values of Row NUCs are determined accordingly.

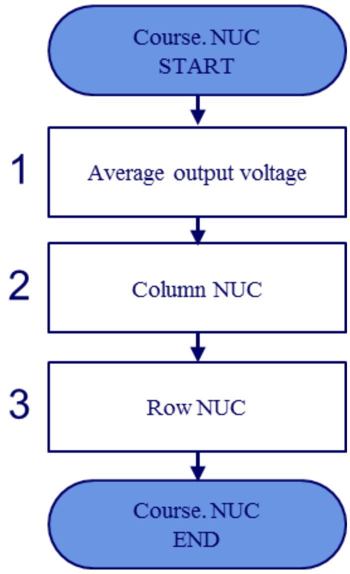


Figure 22 A process flow chart of coarse NUC

- Vskim setting

Modulate the voltage of Vskim so that the average output voltage of 640x480 active cells should be equal to the voltage of DR/2. Determine the voltage of Vskim, which is the closest value to the DR/2.

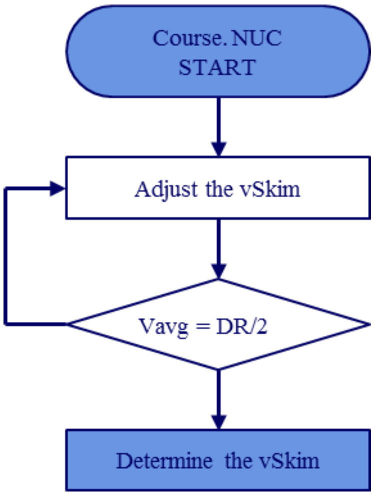


Figure 23 Flow chart for determining the value of vSkim

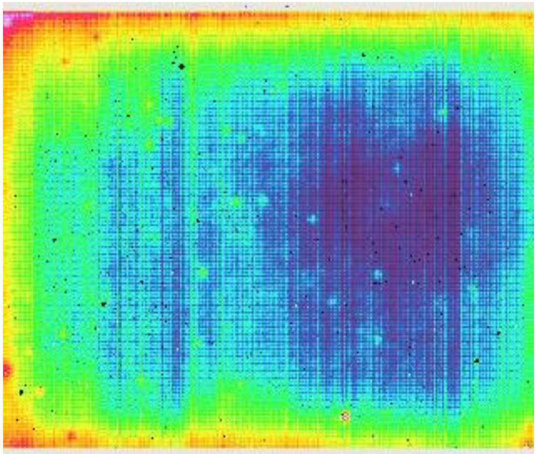


Figure 24 **After setting the average output voltage of active cells to be the voltage of DR/2**

- Auto Vskim setting (recommend)

Flow chart for auto Vskim setting is described below.

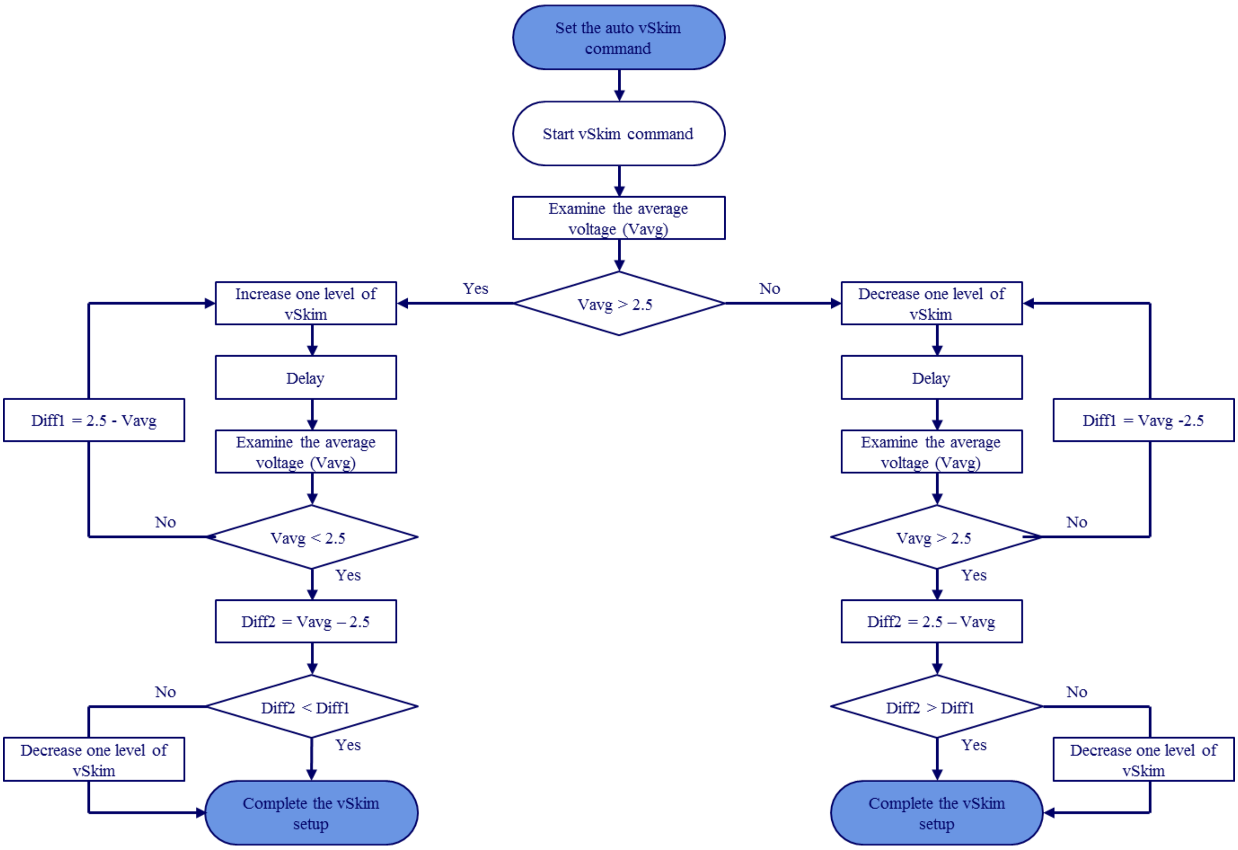


Figure 25 Flow chart for auto setting

- Column NUC setting

Modulate the high value of vBlind so that more than 90% (tunable value) of 640x480 active cells should be over the value of DR/2. Then determine the high value of vBlind.

Adjust the high value(**not low value**) of vBlind so that over 90% of 640x480 active cells should be under the value of DR/2. Then settle the low value of vBlind.

Ref) Because the low value of vBlind can’t directly change the output voltage, the value of vBlind is determined by modulating the high value of vBlind and observing the corresponding output voltage.

Determine NUC value that makes the average voltage in the Column lines close to the value of DR/2, varying each Column NUC bias from 0 to 15.

Ref) The initial value of NUC bias is set to 15. As reducing the NUC bias from 15 to 0, find a suitable bias value.

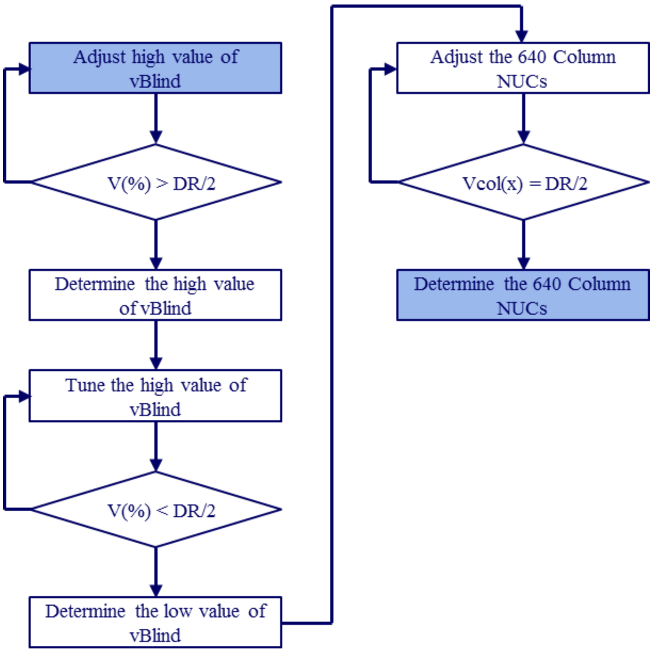


Figure 26 Flow chart for determining the Column NUCs

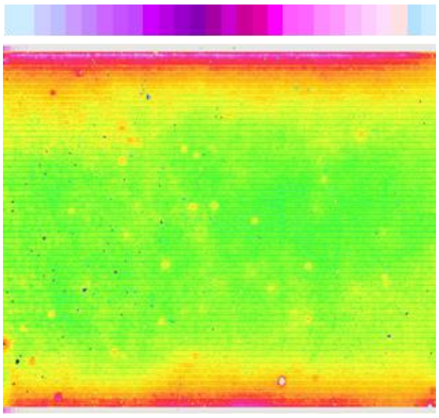


Figure 27 After setting the 640 values of Column NUC bias generator

- Row NUC setting (recommend)

Modulate the high value of vBolo so that more than 90% of 640x480 active cells should be over the value of DR/2. Then determine the high value of vBolo..

Adjust the high value of vBolo so that over 90% of 640x480 active cells should be under the value of DR/2. Then settle the low value of vBolo.

Ref) Because the low value of vBolo can't directly change the output voltage, the value of vBolo is determined by modulating the high value of vBolo and observing the corresponding output voltage.

Determine NUC value that makes the average voltage in the Row lines close to the value of DR/2, varying each Row NUC bias from 0 to 15.

Ref) The initial value of NUC bias is set to 15. As reducing the NUC bias from 15 to 0, find a suitable bias value.

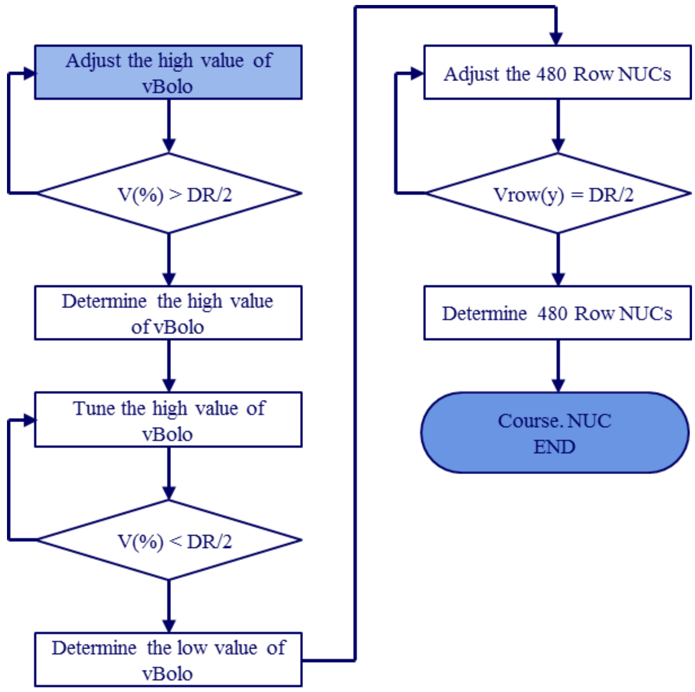


Figure 28 Flow chart for determining the Row NUCs

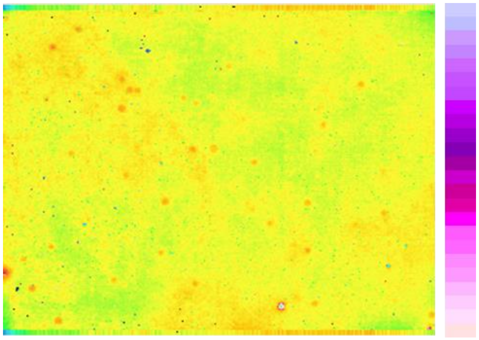


Figure 29 **After settling 480 the values of Row NUC bias generator**

5. PHYSICAL INTERFACE DATA

The packaging has the following traits: vacuum sealed miniaturized ceramic packaging, on-chip(on ROIC) and off-chip(on ceramic package. more precise, recommended) temperature sensor.

5.1 Mechanical interface data

The general mechanical description and the outline dimensions of the DB640-17C-A are presented in the annex. All dimensions are given in millimeters at room temperature.

5.2 Thermal interface data

5.2.1 Operating temperature

The DB640-17C-A guarantee to operate in ambient temperature range from -40°C to +65°C. But, operating and storage at high temperature decreases the vacuum lifetime.

5.2.2 On-chip (at the FPA level) thermometer

An on-chip thermometer provides an analog output voltage related to the temperature of FPA. The output voltage range is 1.75 ~ 2.05V [315mV] related to -40 ~ 65°C [105°C], As a consequence, on-chip thermometer has a characteristic of 3mV/K. But there is a manufactural variation rising a offset between an absolute temperature value and an measured one. The value is useful only as a reference.

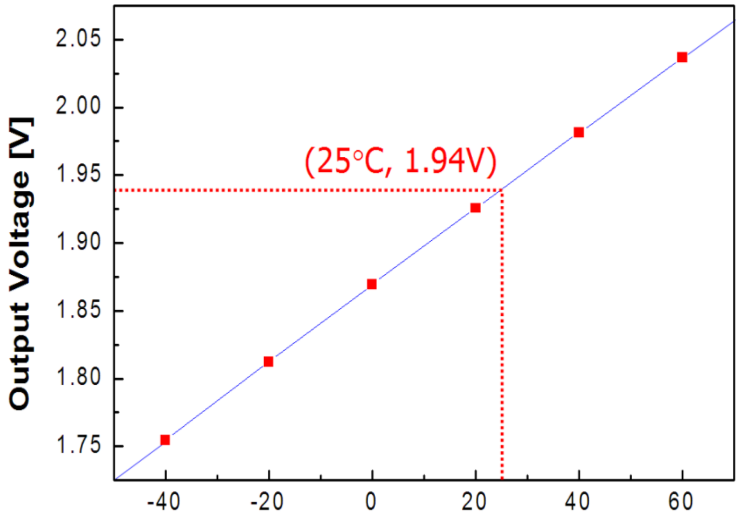


Figure 30 Characteristic of On-chip thermometer

To activate the on-chip thermometer, trim resister value of ‘Temp row output’ (see Table 5 ‘15h’) should be 0. Both the 481th and 482th row data are the output voltage related with temperature.

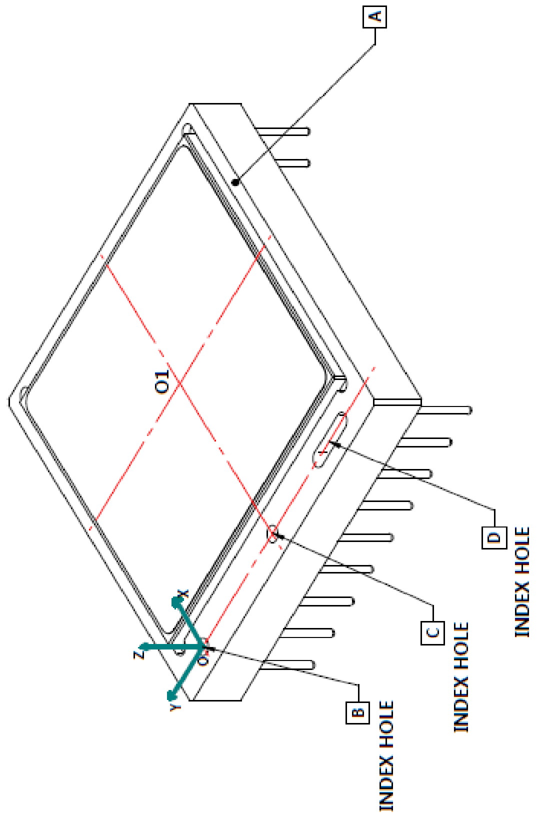
5.3 Optical interface data

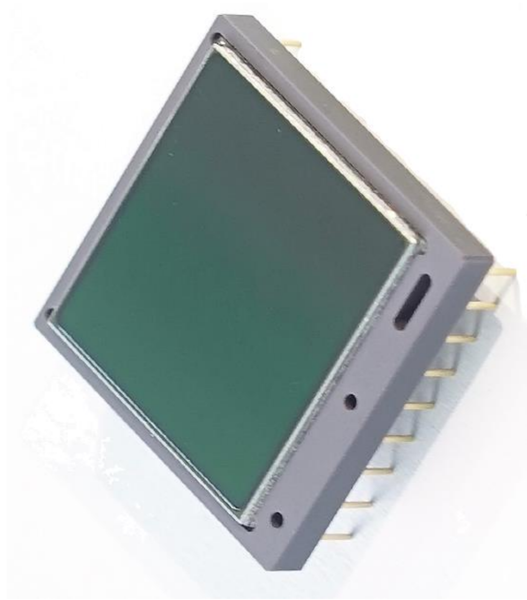
The optical interface is comprised of an infrared window with the antireflective coating to optimize the incident radiation onto the FPA and a high pass filter to suppress short infrared wavelength (<7.5 μm). It is made from silicon with a thickness of 0.7 mm. The detailed optical interface is presented in the annex, sheet 03/04.

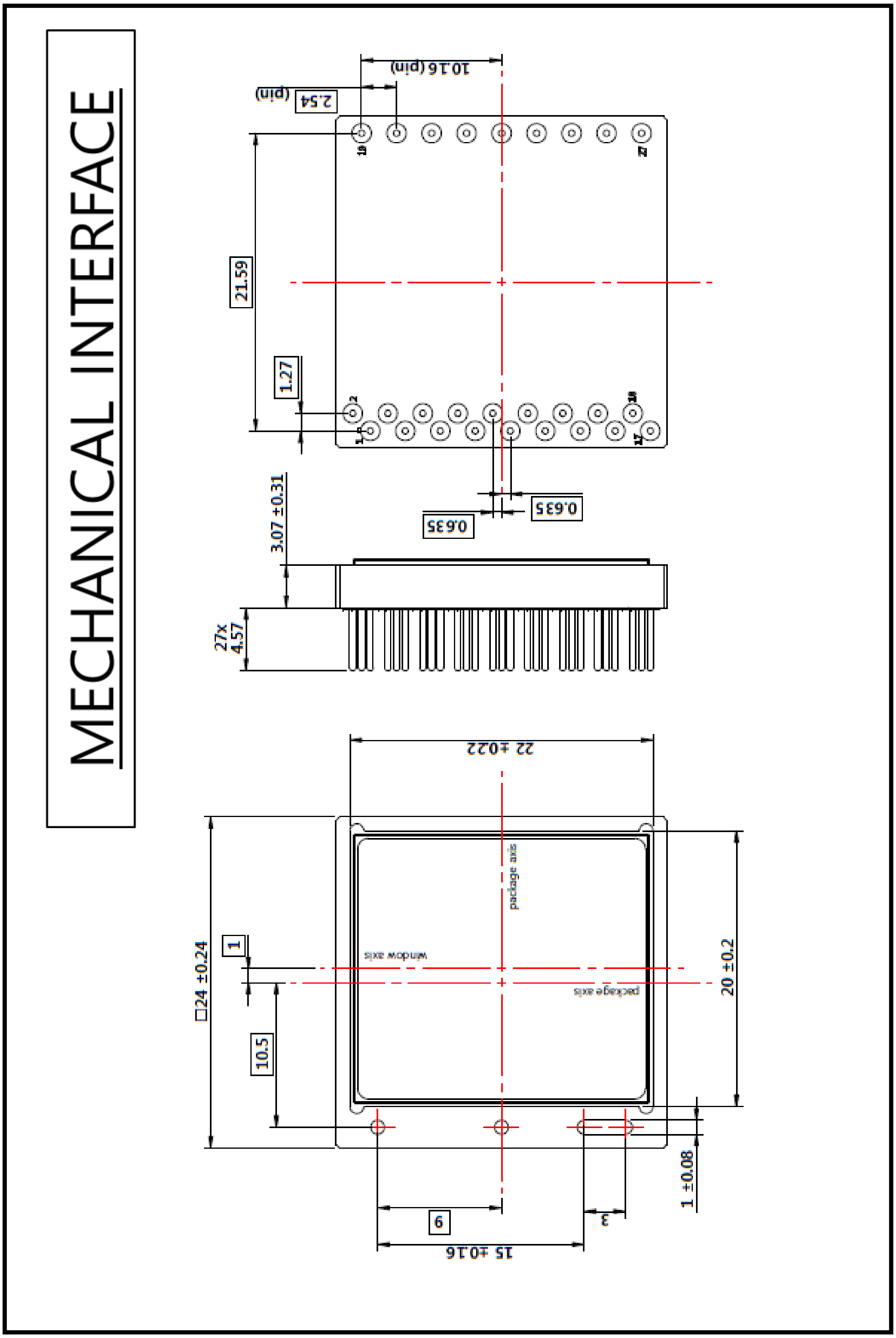
6. ANNEXES

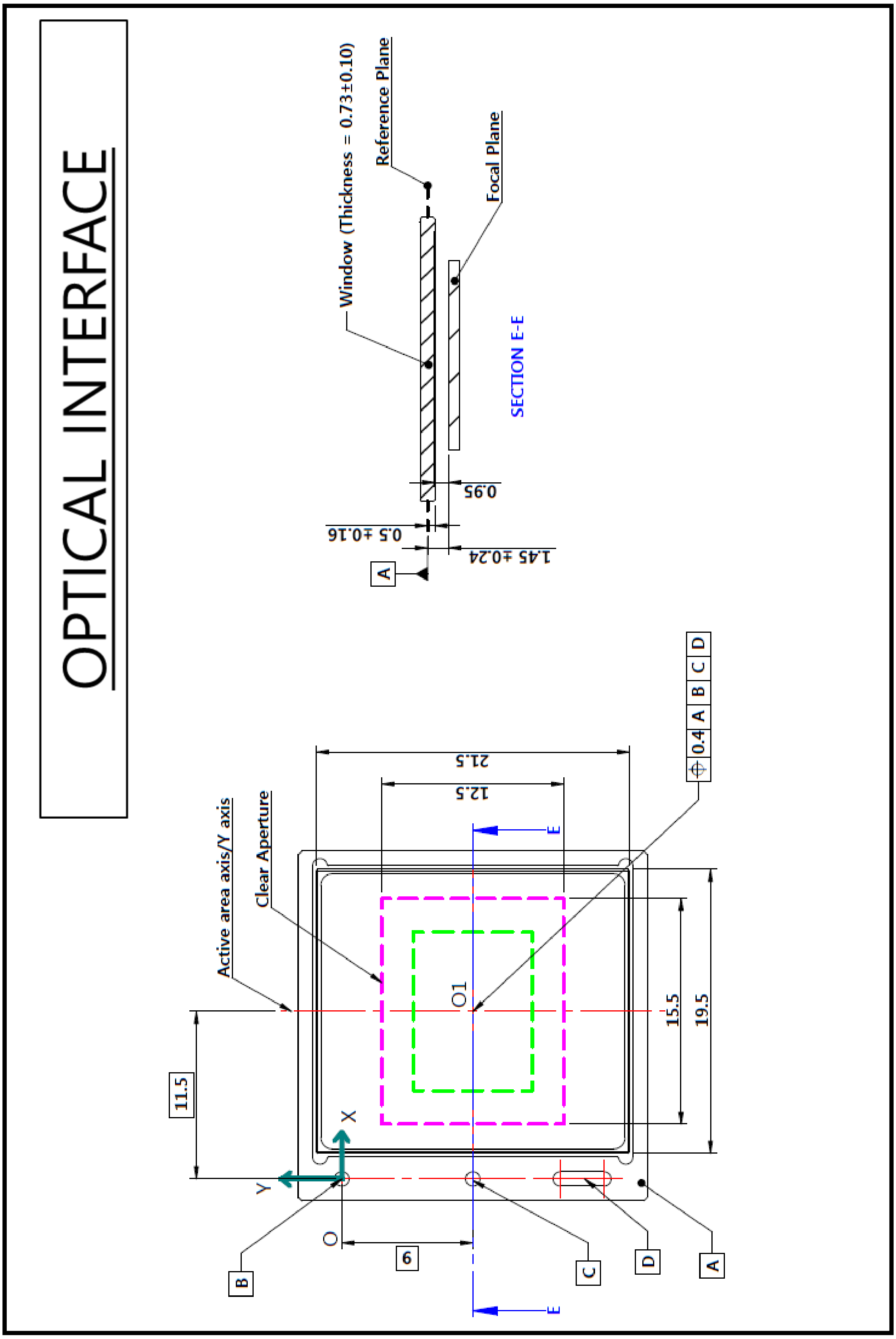
- ✓ General view : sheet 1/4
- ✓ Mechanical interface: sheet 2/4
- ✓ Optical interface: sheet 3/4
- ✓ Electrical interface: sheet 4/4

GENERAL VIEW



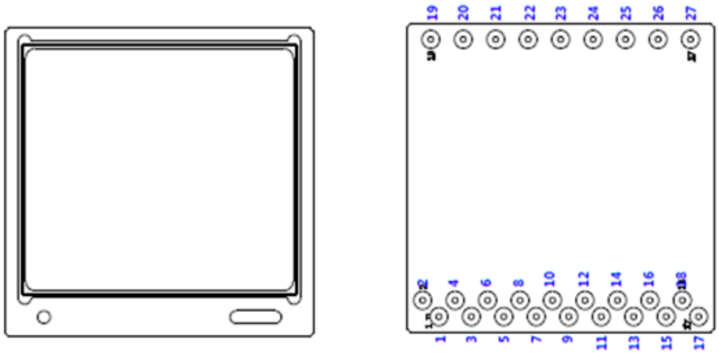



MECHANICAL INTERFACE
10.16 (pin)
2.54 (pin)
21.59
1.27
0.635
0.635
3.07 ±0.31
27x
4.57
22 ±0.22
□24 ±0.24
1
10.5
window axis
package axis
package axis
20 ±0.2
1 ±0.08
6
3
15 ±0.16


OPTICAL INTERFACE
Window (Thickness = 0.73±0.10)
Reference Plane
Focal Plane
SECTION E-E
0.95
0.5 ±0.16
1.45 ±0.24
A
Active area axis/Y axis
Clear Aperture
21.5
12.5
0.4 A B C D
E
O1
15.5
19.5
11.5
X
Y
O
6
B
C
D
A
E

ELECTRICAL INTERFACE

Pin No.	Function
1	OVDD
2	OGND
3	VOUT_O
4	VOUT_E
5	AVDD1
6	AGND1
7	Reserved
8	AMON
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	ACDD2
15	AGND2
16	Reserved
17	TEMP_1
18	TEMP2



Pin No.	Function
19	DVDD1
20	DGND1
21	FSYNC
22	LSYNC
23	MCLK
24	DVDD2
25	DGND2
26	CLE
27	SCDI

7. GLOSSARY

FPA : Focal Plane Array
MCLK : Master Clock
NETD : Noise Equivalent Temperature Difference
ROIC : Read-Out Integrated Circuit
TCR : Temperature Coefficient of Resistance
TEC : ThermoElectric Cooler (Peltier module)
VOUT_O : Odd Row Output Voltage
VOUT_E : Even Row Output Voltage
AVDD : Analog Supply Voltage
DVDD : Digital Supply Voltage
OVDD : Output Supply Voltage
AGND : Analog Ground
DGND : Digital Ground
DGND : Output Ground
SCDI : Serial Communication Data Input
CDS : Correlated Double Sampling

8. LIST OF FIGURES

9. LIST OF TABLES