

Applications

- Single-ended and Push-pull Optical Receivers
- Low-noise Drop Amplifiers
- Distribution Amplifiers
- Multi-Dwelling Units
- Single-ended Gain Block

Product Features

- Gain, return loss and bias externally adjustable
- On-chip active bias for consistent bias current and repeatable performance
- DC – 2000 MHz bandwidth
- Low noise: typical NF < 2 dB to 1000MHz
- Flexible 5 V to 8 V biasing
- $I_{DD} = 120$ mA typical at V_{DD} 5V in application circuit
- 19 dB typical gain in application circuit
- +40 dBm typical OIP3
- +61 dBm typical OIP2
- +21 dBm typical P1dB
- Low distortion: CSO -66 dBc, CTB -78 dBc
- (10 dBmV/ch at input, 80 ch NTSC flat)
- pHEMT device technology
- SOT-89 package

General Description

The TAT7457 is a low cost RF amplifier designed for applications from DC to 2000 MHz. The balance of low noise and distortion provides an ideal solution for a wide range of broadband amplifiers used in cable television applications such as optical receivers and low noise front ends.

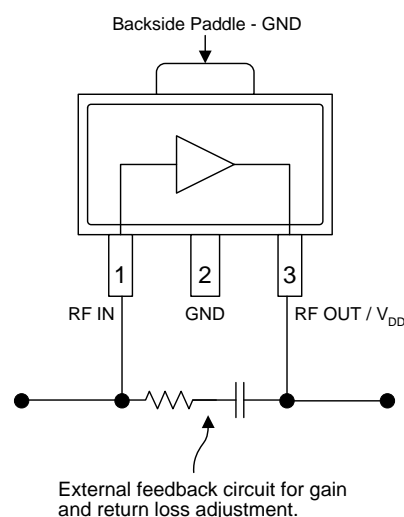
The TAT7457 has features allowing a great deal of design-in flexibility. Gain and return loss are adjustable with an external feedback resistor. An internal bias circuit mitigates the effect of temperature and process variation and an external resistor may be used to adjust the bias current to optimize distortion or noise performance. There are no on-chip capacitors limiting the low freq response which extends down to DC.

The TAT7457 is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost. It provides excellent gain and return loss consistency inherent to the pHEMT process.



SOT-89 Package

Functional Block Diagram



Pin Configuration

Pin No.	Label
1	RF IN
2	GND
3	RF OUT/V _{DD}
Backside Paddle	GND

Ordering Information

Part No.	Description
TAT7457	75 Ω High Linearity pHEMT Amplifier
TAT7457-EB	Assembled Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
Device Voltage (V_{DD})	+10 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD}	5		8	V
I_{DD}		120		mA
Tj for >10 ⁶ hours MTTF			+150	°C

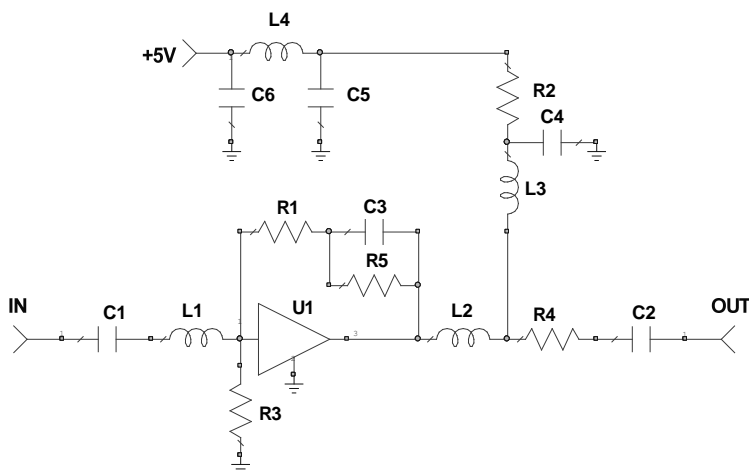
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} =+5 V, Temp= +25°C, Freq.=DC to 1200 MHz

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		DC		1200	MHz
Gain	50-1000 MHz		19		dB
Gain Flatness			+/- 0.7		dB
Noise Figure			2.0		dB
Input Return Loss			18		dB
Output Return Loss			18		dB
Gain	50-1200 MHz		19		dB
Gain Flatness			+/- 0.7		dB
Noise Figure			2.3		dB
Input Return Loss			14		dB
Output Return Loss			17		dB
Output P1dB			+21		dBm
Output IP2	f1=225 MHz, f2=325 MHz Pout = +5 dBm/tone		+61		dBm
Output IP3			+40		dBm
CSO	10 dBmV/channel at input, flat loading, 80 channels NTSC+QAM upto 1218 MHz.		-66		dBc
CTB			-78		dBc
Thermal Resistance, θ_{jc}	Junction to case		38		°C/W

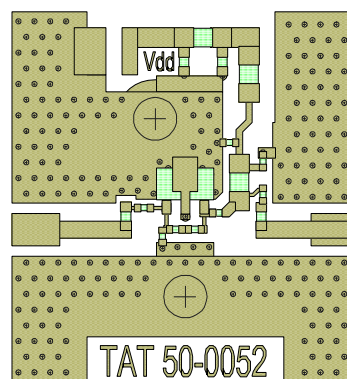
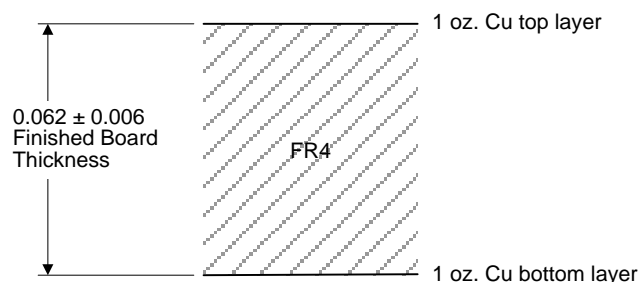
Reference Design – DC-1200 MHz



Bill of Material

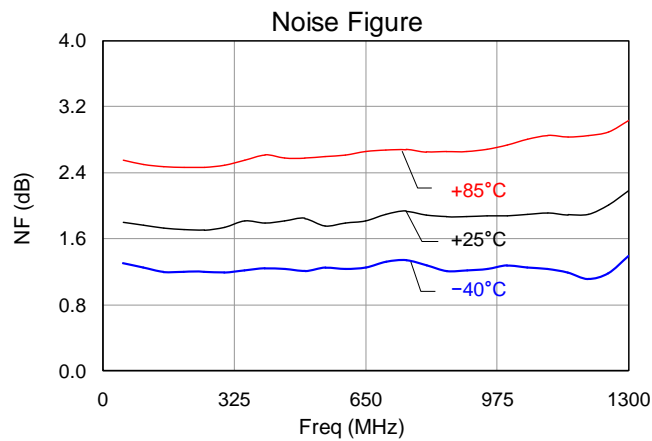
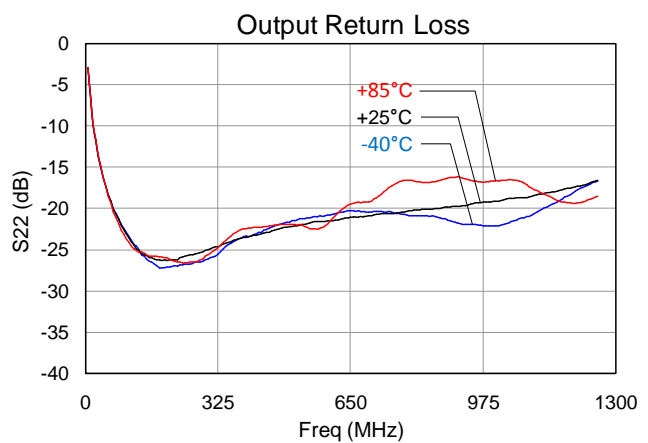
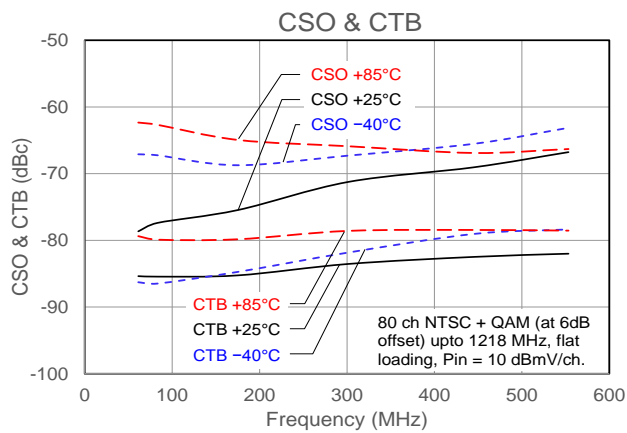
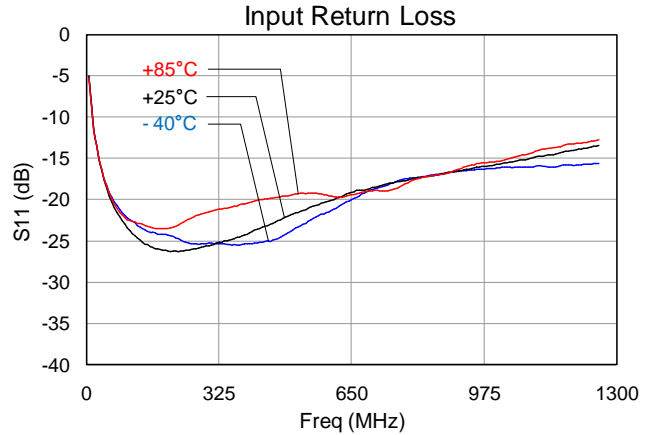
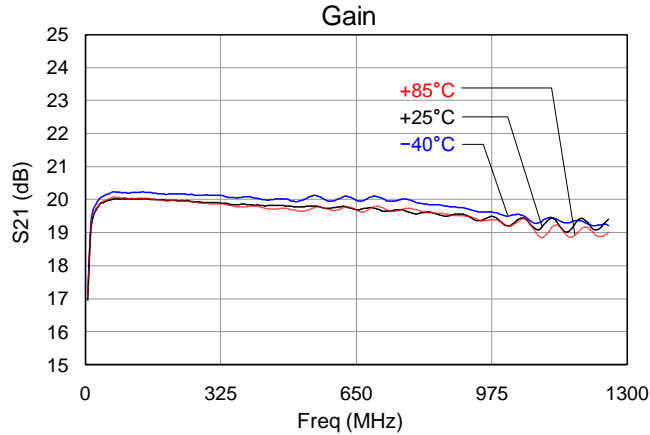
Reference	Value	Description	Manuf.	Part Number
U1		Amplifier, SOT-89	TriQuint	TAT7457
R1	1 k Ω	Thick Film Res., 0402, 1%	various	
R2	0 Ω	Thick Film Res., 1206	various	
R3	N/L			
R4	0 Ω	Thick Film Res., 0402	various	
R5	75 k Ω	Thick Film Res., 0402, 1%	various	
C1, C2	0.01 μ F	Ceramic Cap, 0603, X7R, 16V, 10%	various	
C3, C4	0.01 μ F	Ceramic Cap, 0402, X7R, 16V, 10%	various	
C5, C6	0.1 μ F	Ceramic Cap, 0603, X7R, 16V, 10%	various	
L1, L2	4.7 nH	Ceramic Wire-Wound Ind, 0402, 5%	various	
L3	880 nH	Ferrite Ind., Vertical Wire-Wound, 1206, 10%	various	
L4	910 nH	Ferrite Ind., Vertical Wire-Wound, 1008, 10%	various	

Evaluation Board PCB Stack Up and Material



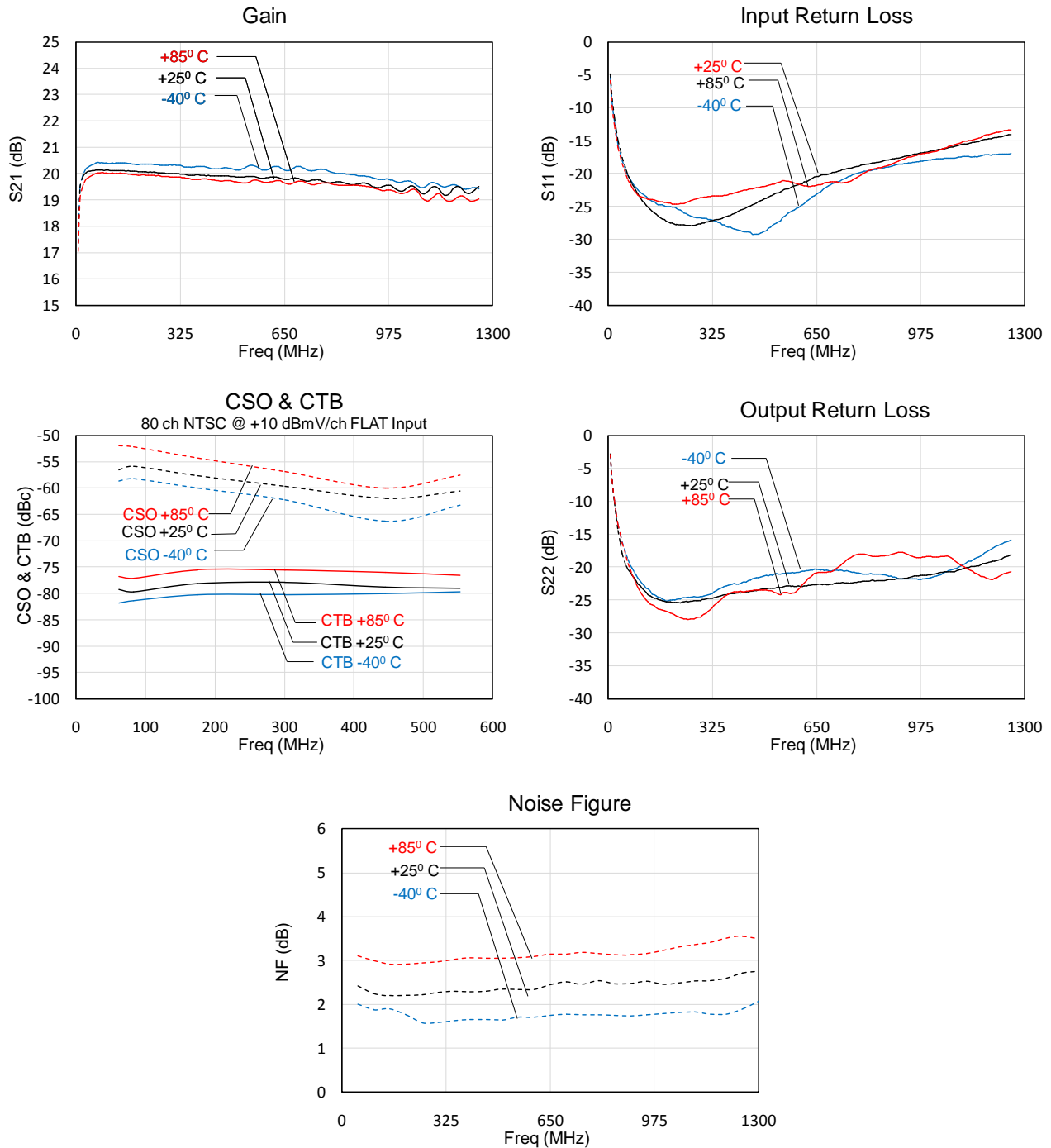
Performance Plots – $V_{DD} = +5$ V

Test conditions unless otherwise noted: $V_{DD} = +5$ V, $I_{DD} = 120$ mA (typ.)

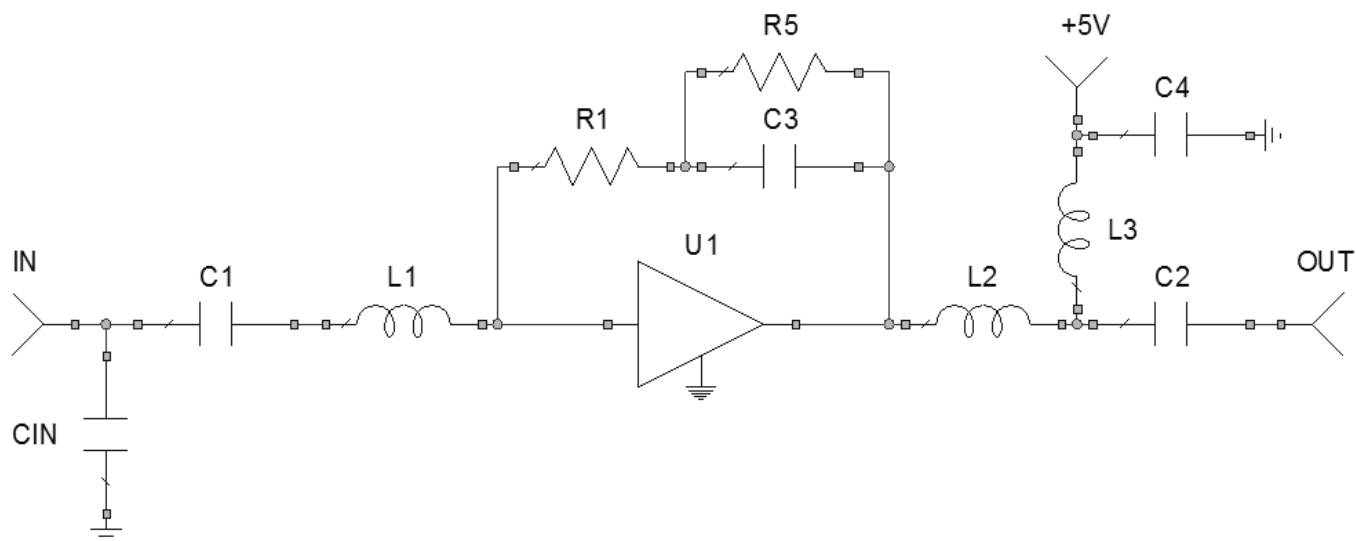


Performance Plots – $V_{DD} = +8\text{ V}$

Test conditions unless otherwise noted: $V_{DD} = +8\text{ V}$, $I_{DD} = 140\text{ mA}$
 I_{DD} adjusted with an external supply, similar to adjusting R3 and R5.



Reference Design – 2.0 GHz Satellite

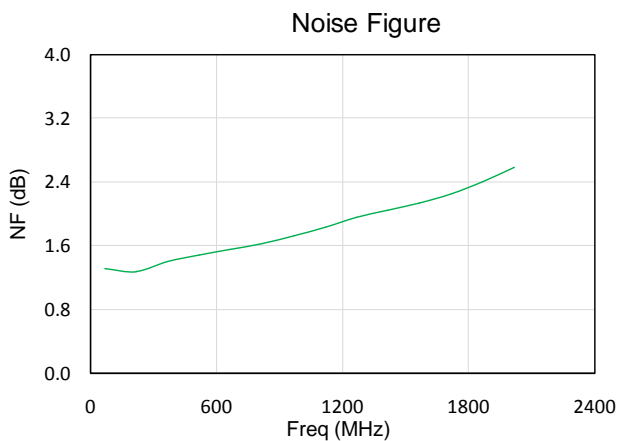
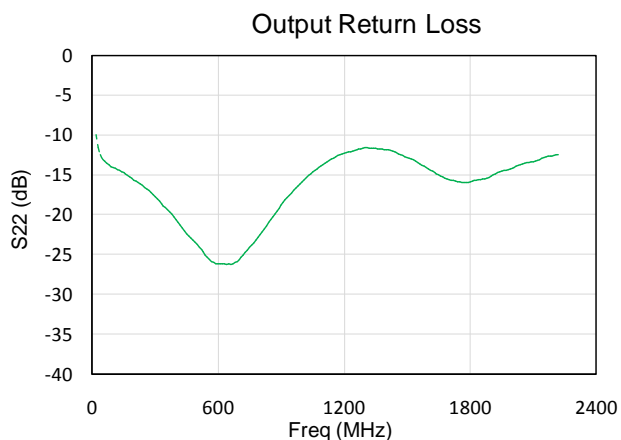
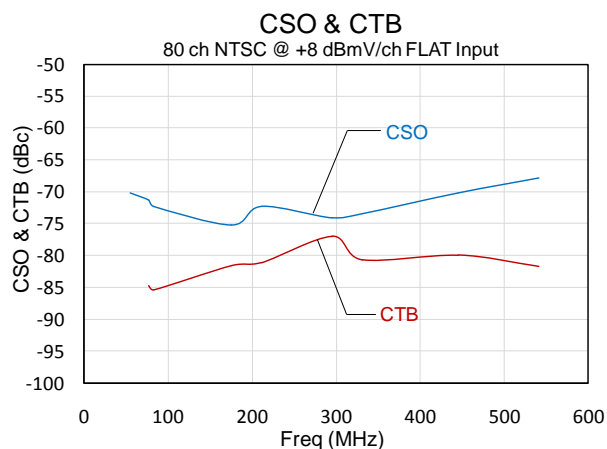
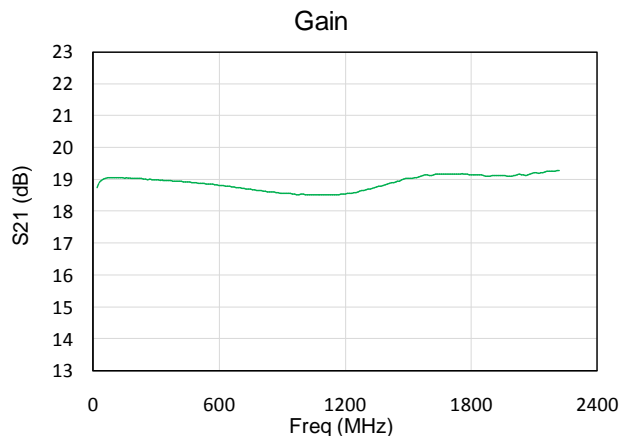


Bill of Material – 2.0 GHz Satellite

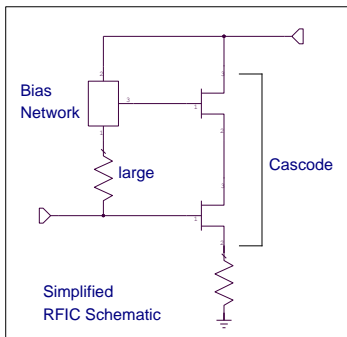
Reference	Value	Description	Manuf.	Part Number
U1		Amplifier, SOT-89	TriQuint	TAT7457
R1	750 Ω	Thick Film Res., 0402, 1%	various	
R5	75 k Ω	Thick Film Res., 0402, 1%	various	
C1, C2	0.01 μ F	Ceramic Cap, 0603, X7R, 16V, 10%	various	
C3	560 pF	Ceramic Cap, 0402, X7R, 16V, 10%	various	
C4	0.01 μ F	Ceramic Cap, 0402, X7R, 16V, 10%	various	
CIN	0.5 pF	Ceramic Cap, 0603, \pm 1 pF	various	
L1	2.7 nH	Ceramic Wire-Wound Ind, 0402, 5%	various	
L2	2.0 nH	Ceramic Wire-Wound Ind, 0402, 5%	various	
L3	880 μ H	Ferrite Ind., Vertical Wire-Wound, 1206, 10%	various	

Performance Plots – 2.0 GHz Satellite

Test conditions unless otherwise noted: $V_{DD}=+5$ V, $I_{DD}=120$ mA (typ.), Temp=+25°C



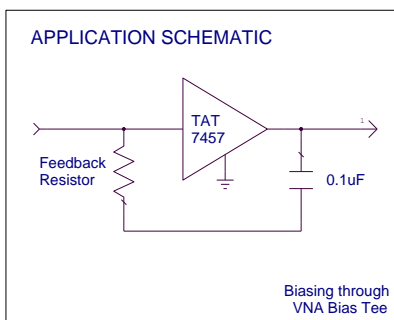
Detailed Device Description



The TAT7457 was designed to be a low cost general purpose amplifier suitable for a wide range of applications.

The TAT7457 is a high gain cascode amplifier with no internal shunt feedback.

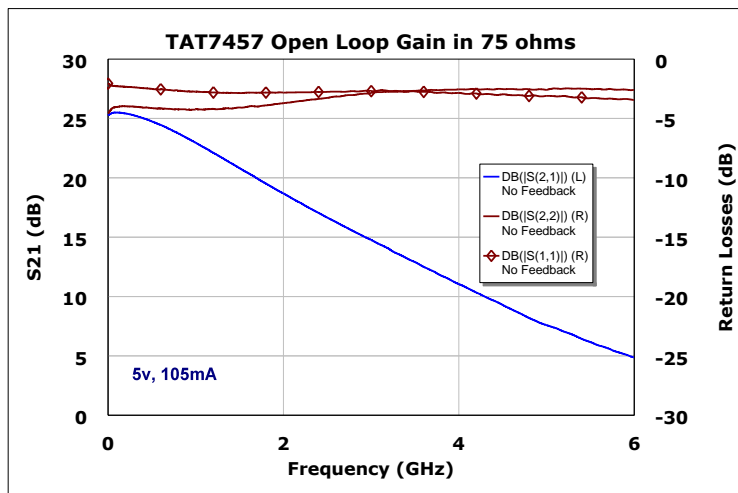
An on-chip biasing network sets the operating conditions for the FETs. This network stabilizes bias current against changes in temperature as well as against the normal process variations expected from wafer to wafer. Stabilized bias current will lead to more consistent RF performance.



Customers may set the gain and return loss of their amplifier by selecting an appropriate external feedback resistor.

Reducing the value of the feedback resistor will reduce the gain and lower the input and output impedances.

Low noise TIA designers may set the value of feedback to a high value (>1k ohm) for best performance.



There are no on-chip capacitors that limit the low frequency response, enabling the TAT7457 frequency response to extend to DC. The open loop gain (no external feedback) and high frequency gain performance is shown in the plot to the left.

Biasing Options for Improved Performance

Distortion and noise performance may be optimized with simple changes to the application circuit.

Noise performance may be improved by adding a large resistor R3 of approximately 20 k Ω to ground. This resistor will reduce the bias current and improve noise.

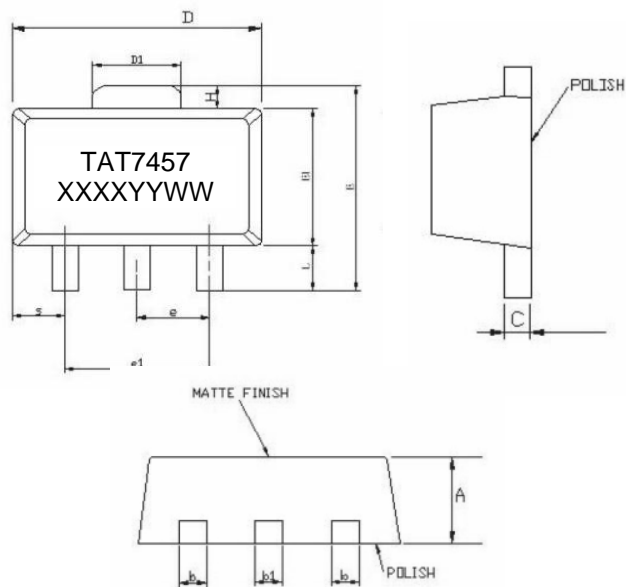
Best distortion occurs on a 6V supply; however for improved distortion on a 5V supply, bias current may be increased by adding a large pull up resistor R5 of approximately 75 k Ω in parallel with the feedback capacitor.

Package Marking and Dimensions

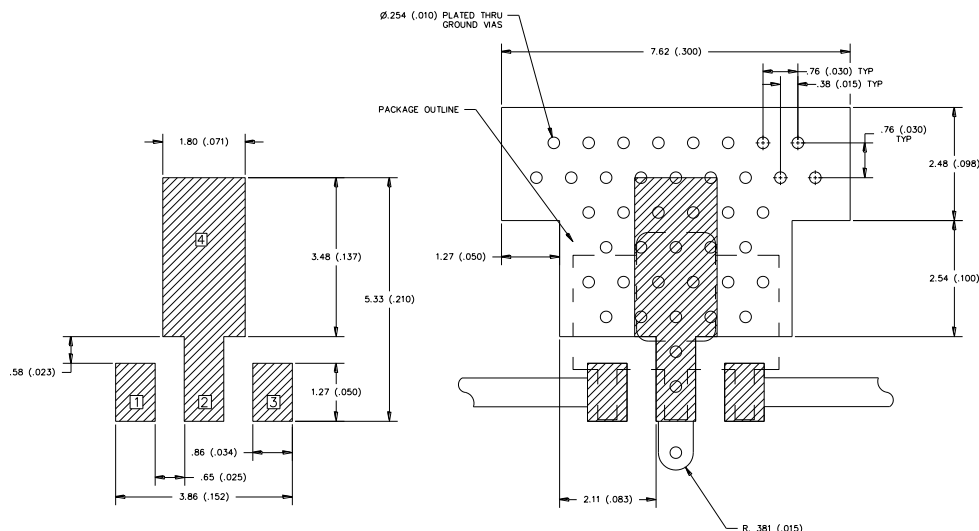
Marking: Part Number – TAT7457

Lot code – XXXXYYWW

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	0.055	0.059	0.063
L	0.89	1.04	1.20	0.0350	0.041	0.047
b	0.36	0.42	0.48	0.014	0.016	0.018
b1	0.41	0.47	0.53	0.016	0.018	0.020
C	0.38	0.40	0.43	0.014	0.015	0.017
D	4.40	4.50	4.60	0.173	0.177	0.181
D1	1.40	1.60	1.75	0.055	0.062	0.069
E	3.64	—	4.25	0.143	—	0.167
E1	2.40	2.50	2.60	0.094	0.098	0.102
e1	2.90	3.00	3.10	0.114	0.118	0.122
H	0.35	0.40	0.45	0.014	0.016	0.018
S	0.65	0.75	0.85	0.026	0.030	0.034
e	1.40	1.50	1.60	0.054	0.059	0.063



PCB Mounting Pattern



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm (#80/.0135") diameter drill and have a final, plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: Passes ≥ 400 V to < 500 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class III
Value: Passes ≥ 2000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: Annealed matte tin over copper.

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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